

Fig. 1

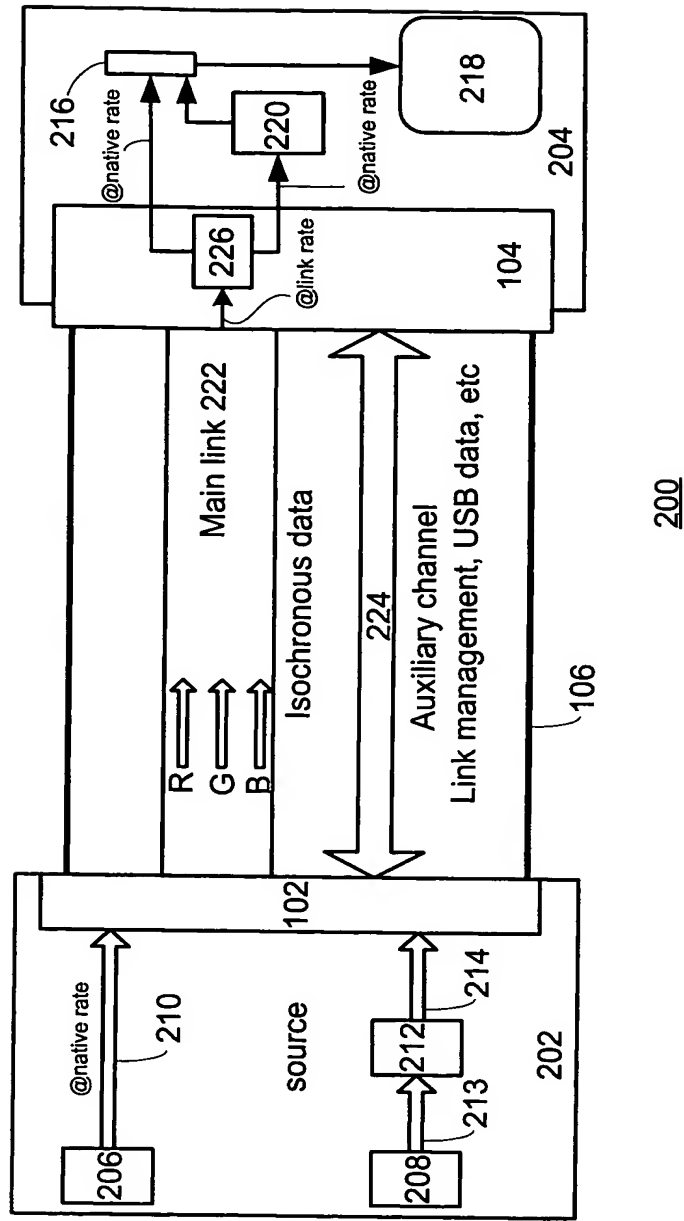


Fig. 2A

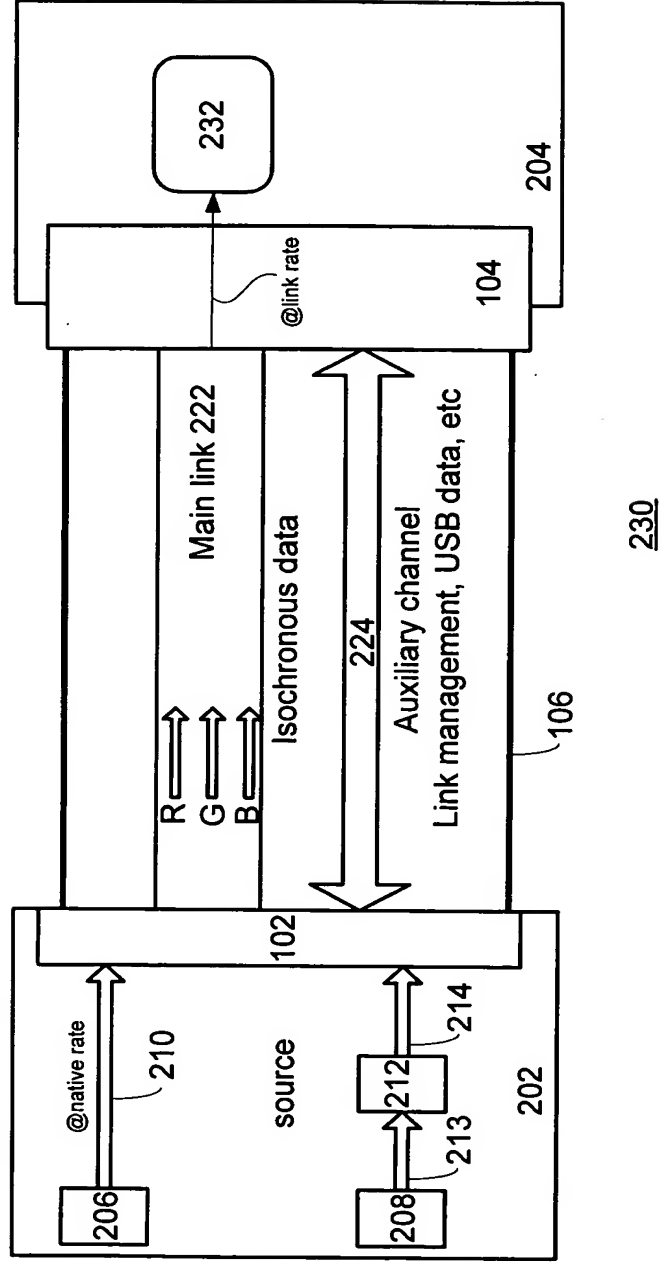


Fig. 2B

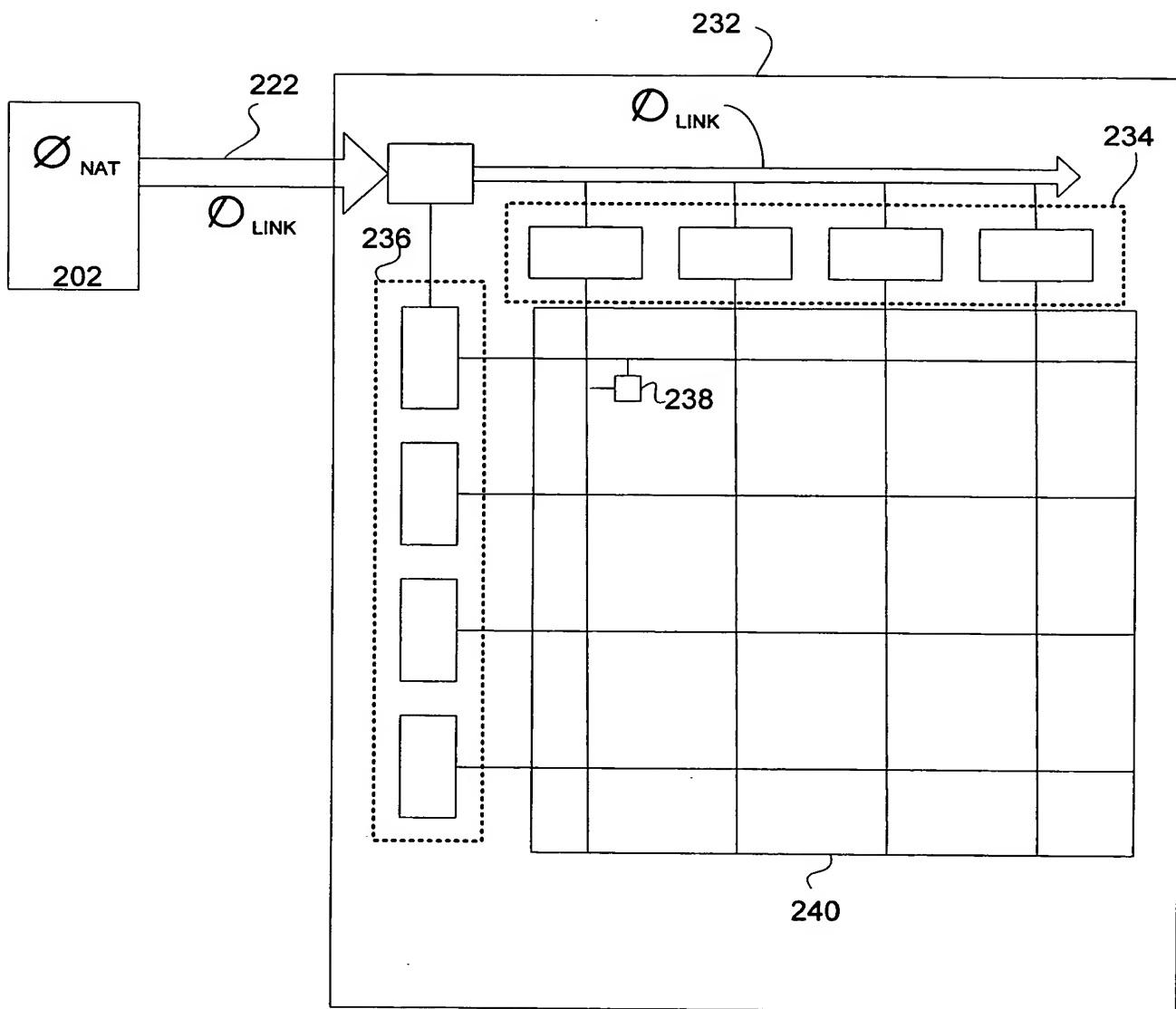


Fig. 2C

### Main Link Data Rates

Nominal Baud Rate per channel (Gbits/second)	Actual Baud Rate per channel (Gbits/second)	Clock Multiplication Factor from 24-MHz crystal
1.0	0.960	x40
1.35	1.344	x56
1.7	1.728	x72
2.1	2.112	x88
2.5	2.496	x104

Fig. 3

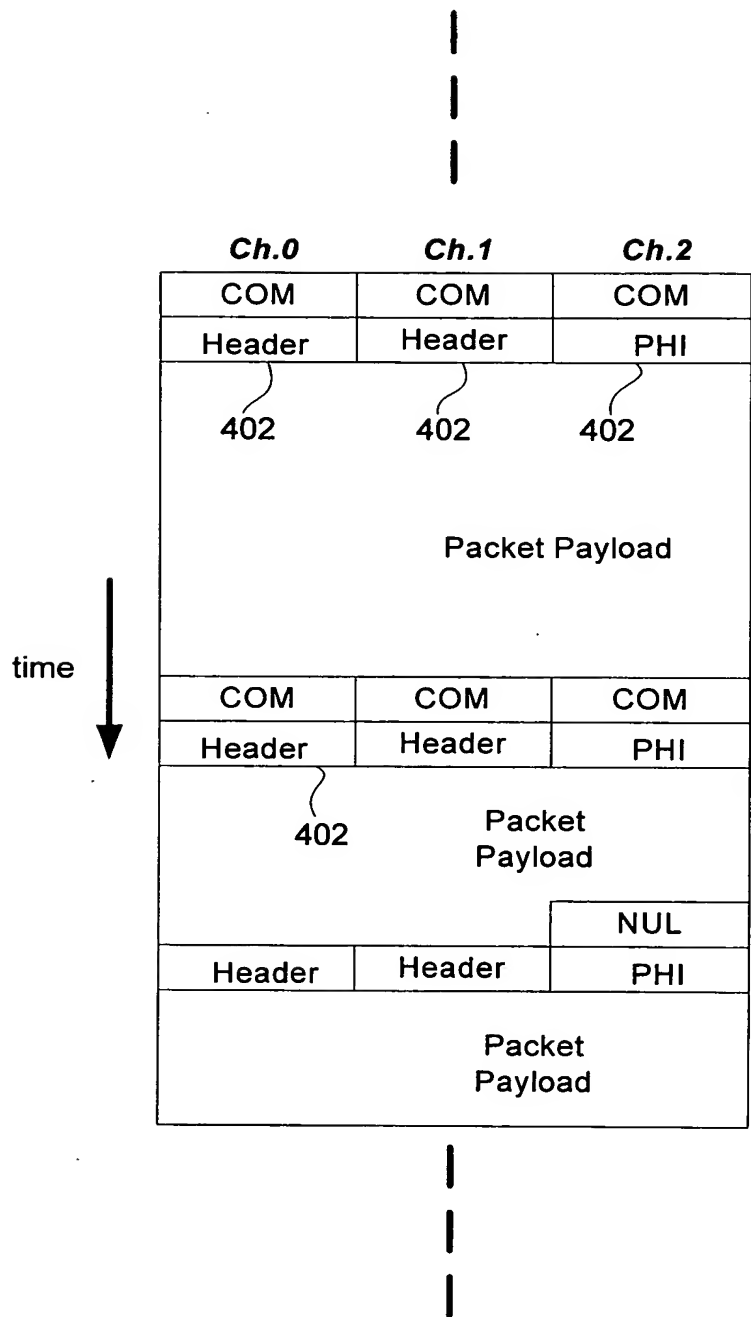


Fig. 4A

Main Link Packet Format

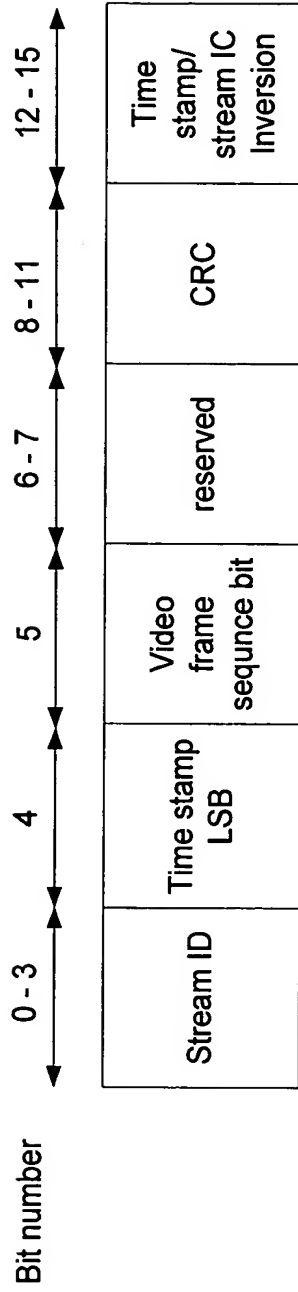


Fig. 4B

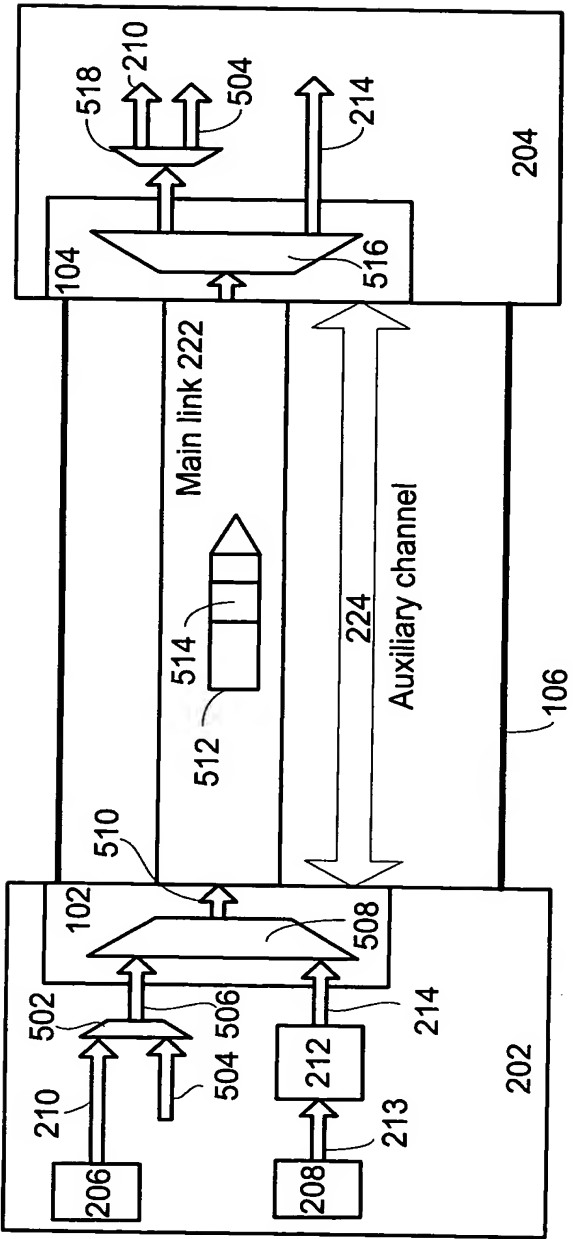
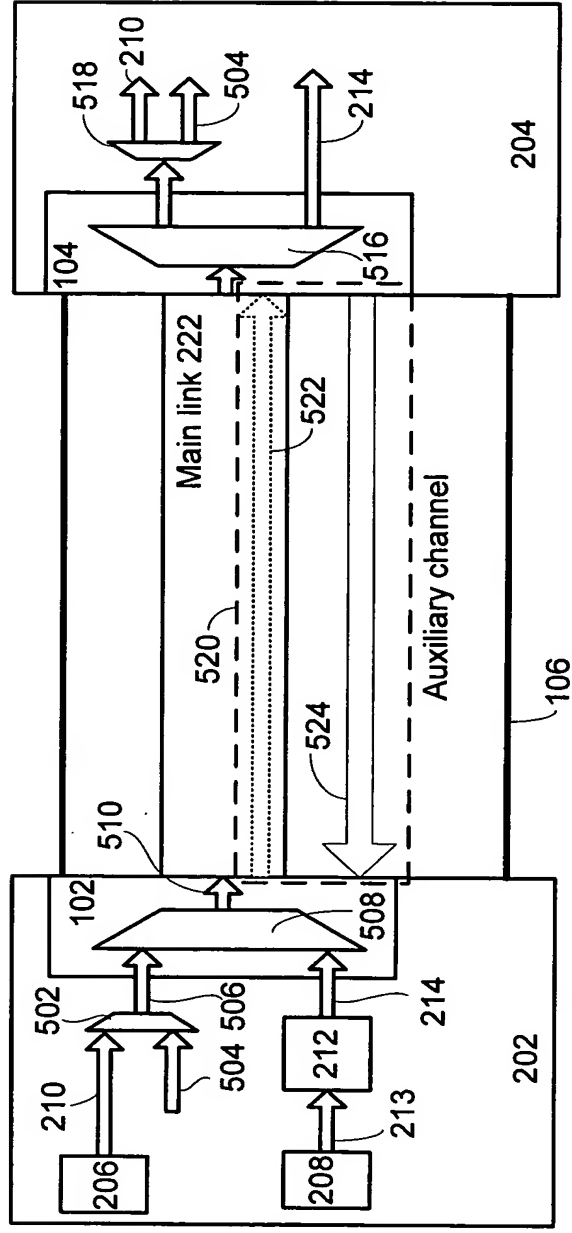


Fig. 5A





500

Fig. 5B

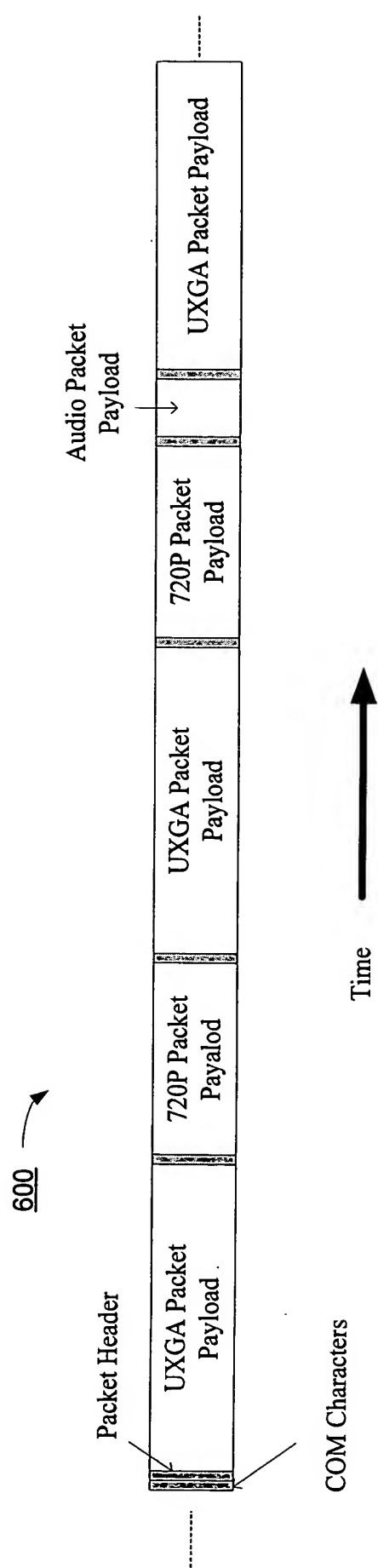


Fig. 6

High-level diagram of link traffic example with three streams

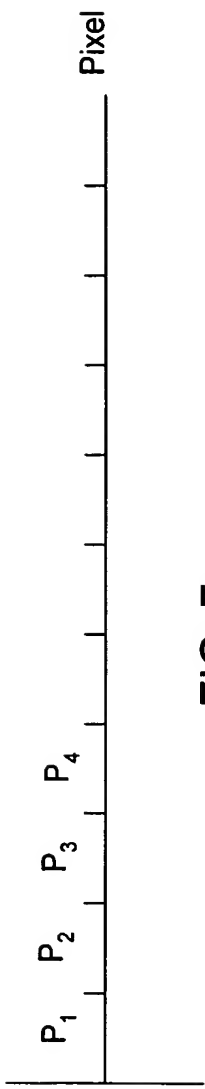
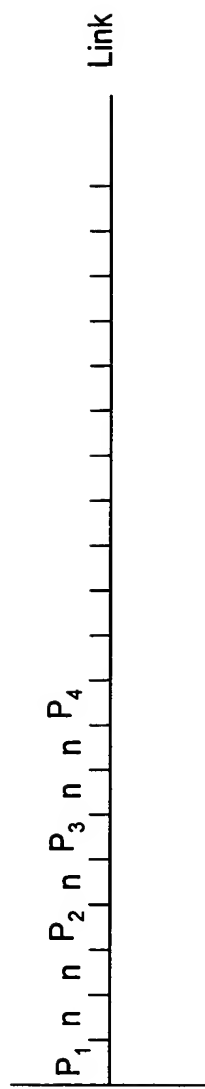


FIG. 7



$n = \text{null}$

FIG. 8

SID = 1		0	0	0	0	CRC	TSP19-16	PHI
Sub-packet Header	902	Sub-packet Header	902	SPS	904			
Sub-packet Payload								
SID = 1	1	0	0	0	CRC	TSP3-0	PHI	
Packet Payload for SID 1								

Fig. 9A

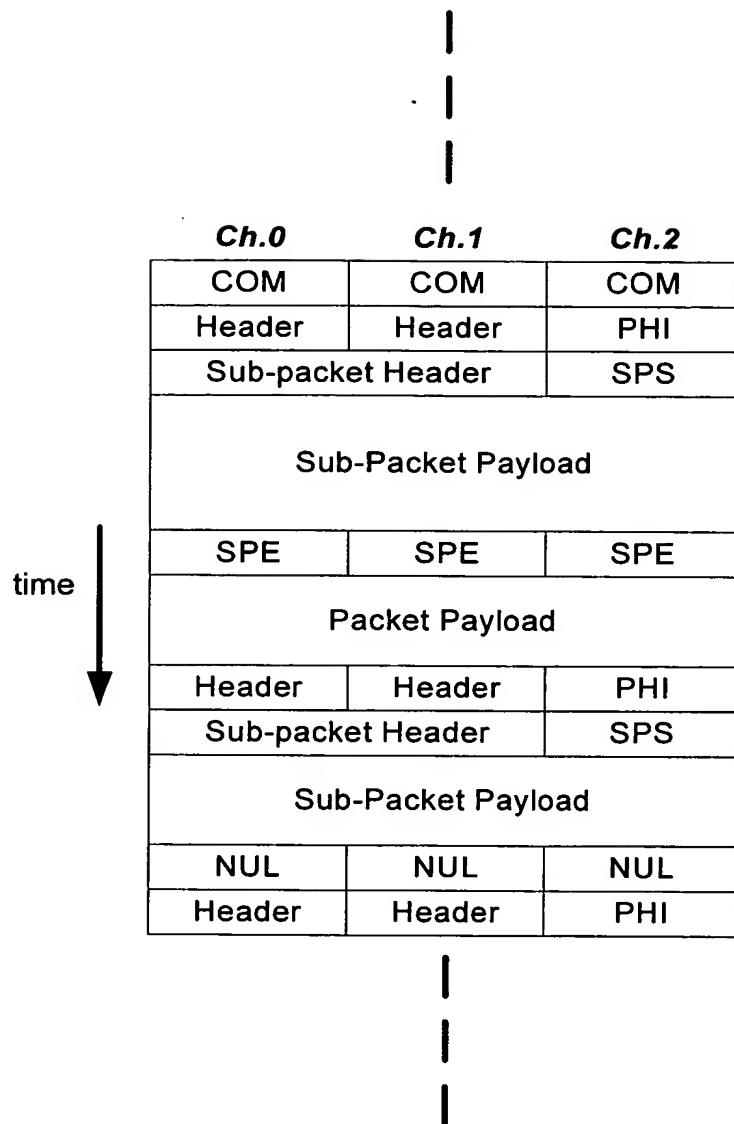


Fig. 9B

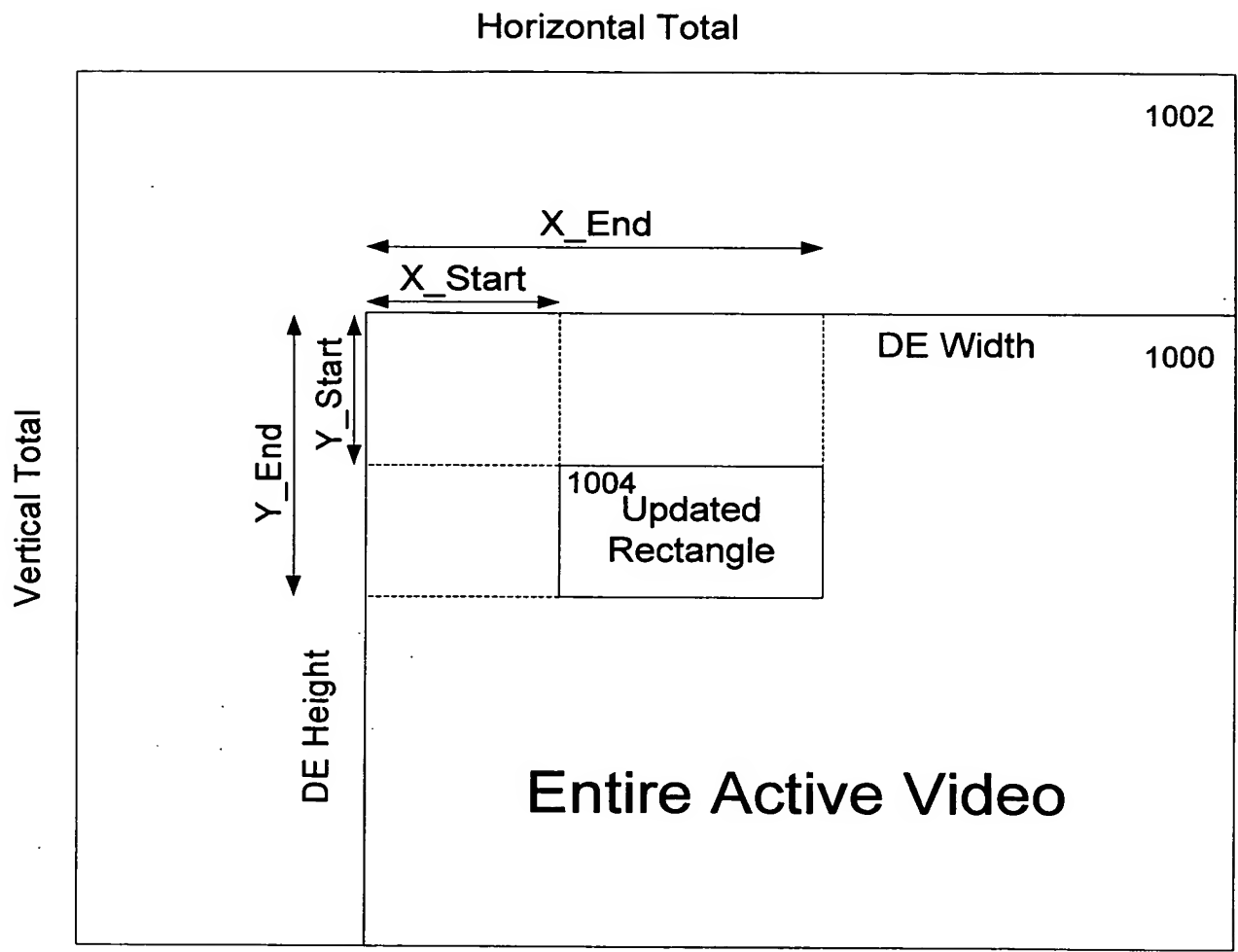


Fig. 10

Phase	Transmitted Link Characters	Binary pattern
1	D10.2	0101010101 0101010101 0101010101 0101010101 0101010101
2	K28.7	0011111000 0011111000 0011111000 0011111000 0011111000
3	K28.5, and three D10.2	0011111010 0101010101 0101010101 0101010101 1100000101

Main Link Training Pattern

Fig. 11

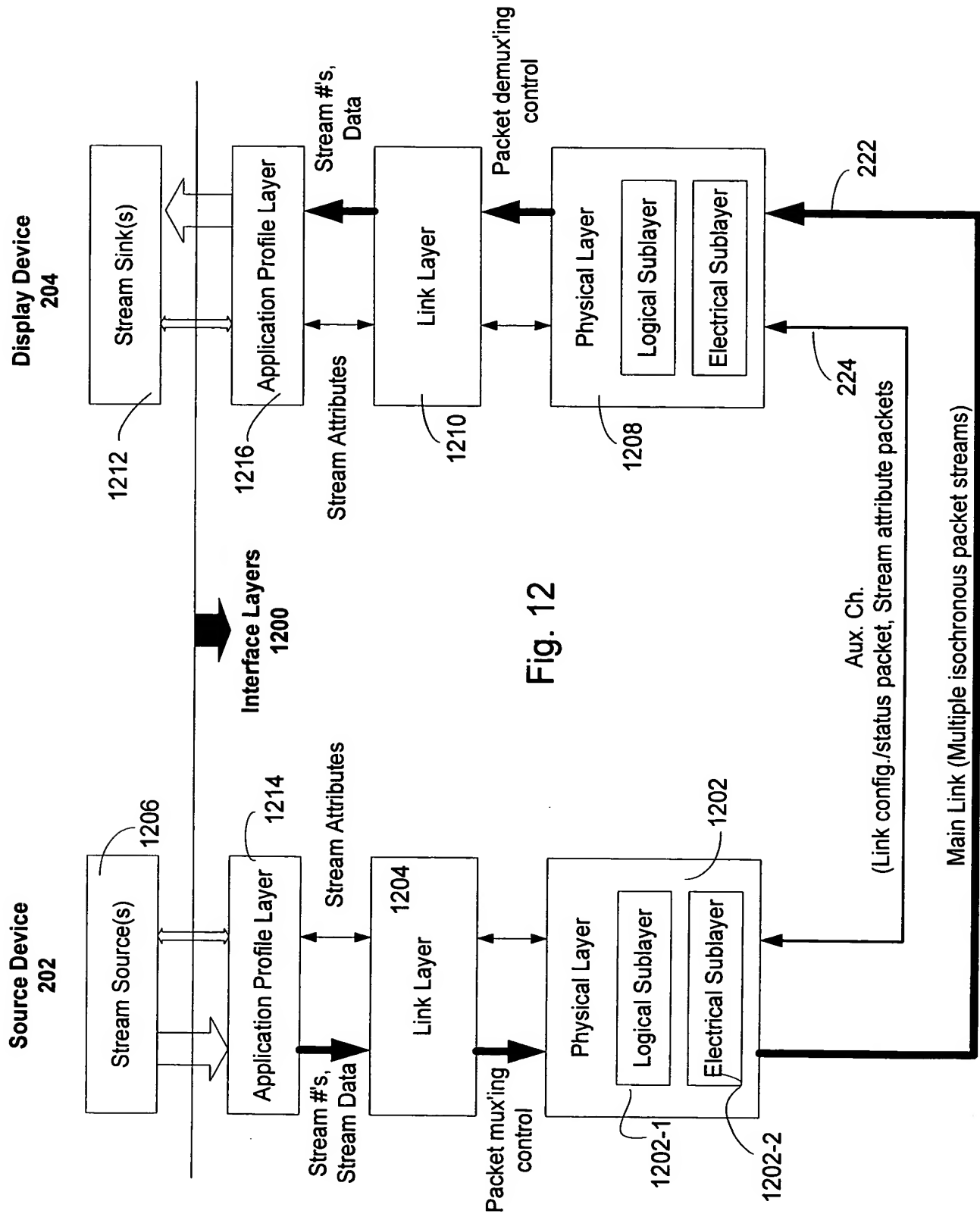


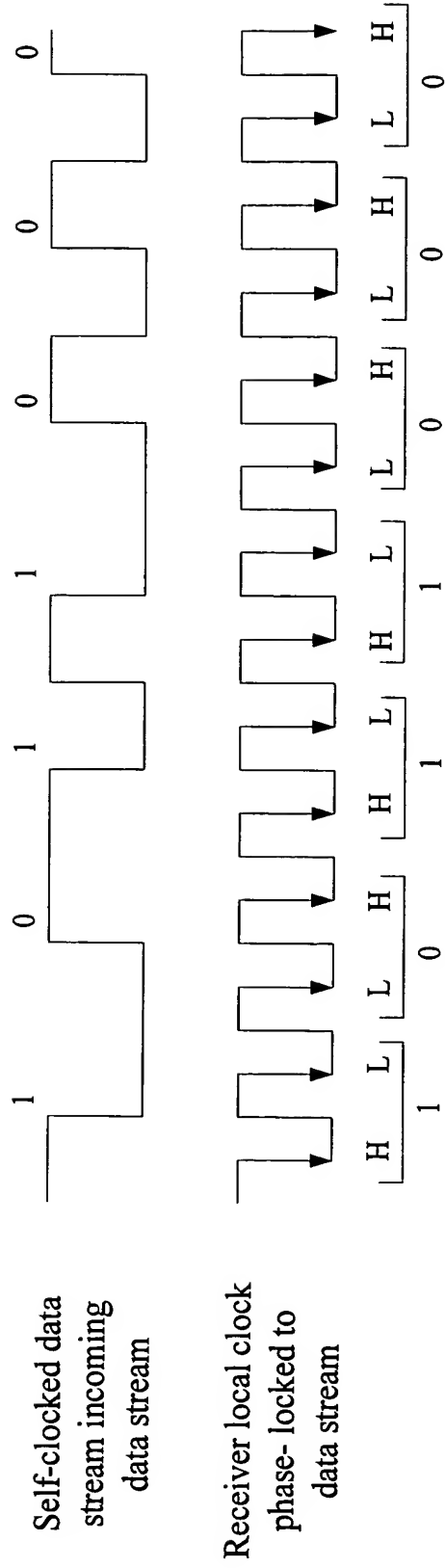
Fig. 12



### 8B/10B Special Characters Usage

Encoding	Name	Description
K28.5	Comma (COM)	Inserted between packets. Also used as part of Test Pattern
K28.7	TrainingPattern (TPN)	Sent during Training Pattern transmission for bit/byte clock lock.
K23.7	Null (NUL)	Sent within the packet period when there is no data to transmit.
K28.2	Sub-packet Start (SPS)	Indicate a start of sub-packet inserted in a packet
K29.7	Sub-packet End (SPE)	Indicate an end of sub-packet inserted in a main packet.
K28.0	PacketHeaderIndicator (PHI)	Sent along with 16 bits of header for header identification.
K28.1		Reserved
K28.3		Reserved
K28.4		Reserved
K28.6		Reserved
K25.7		Reserved
K27.7		Reserved

Fig. 13



A Manchester II-Coded Stream

Fig. 14

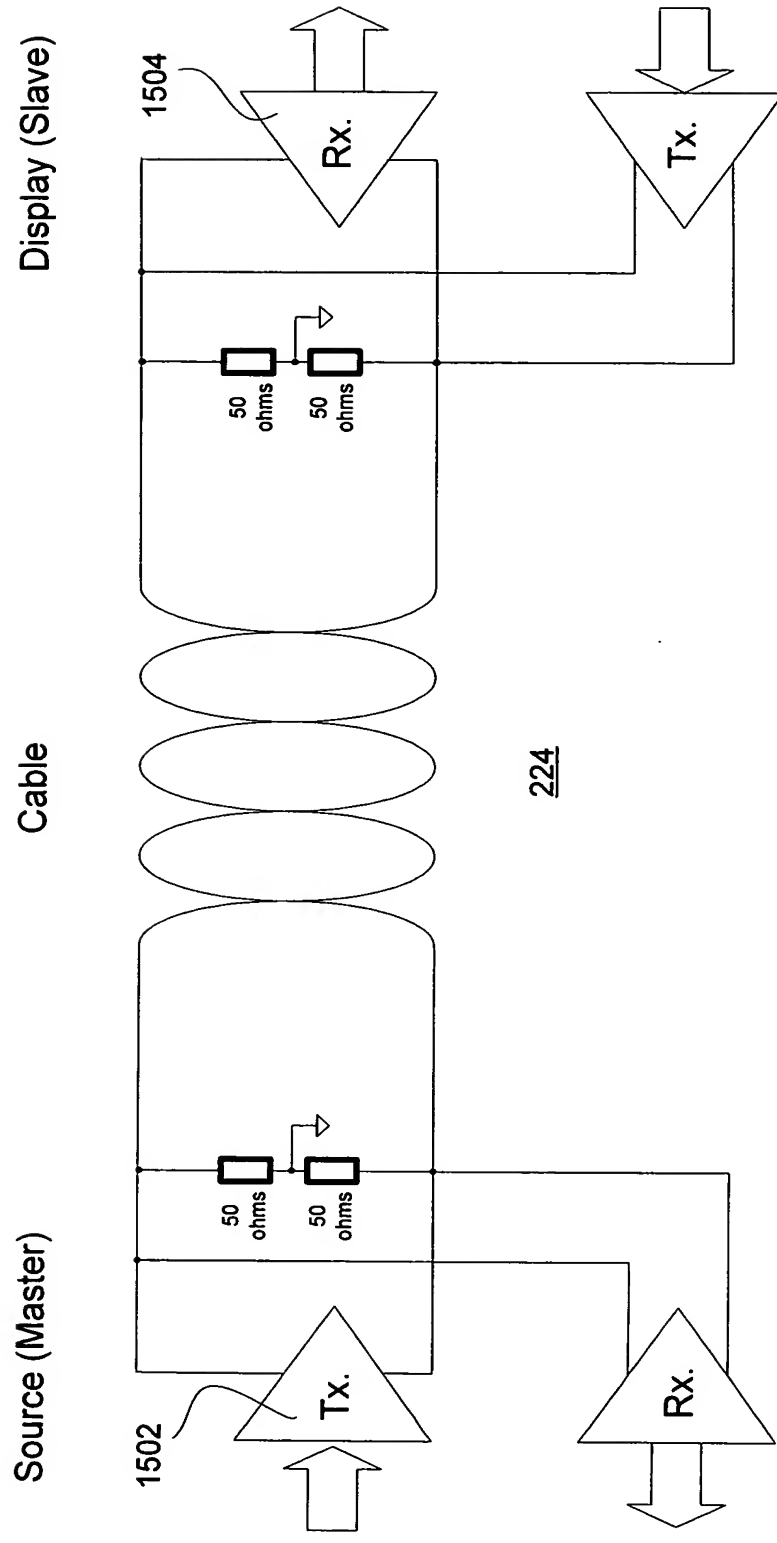


Fig. 15

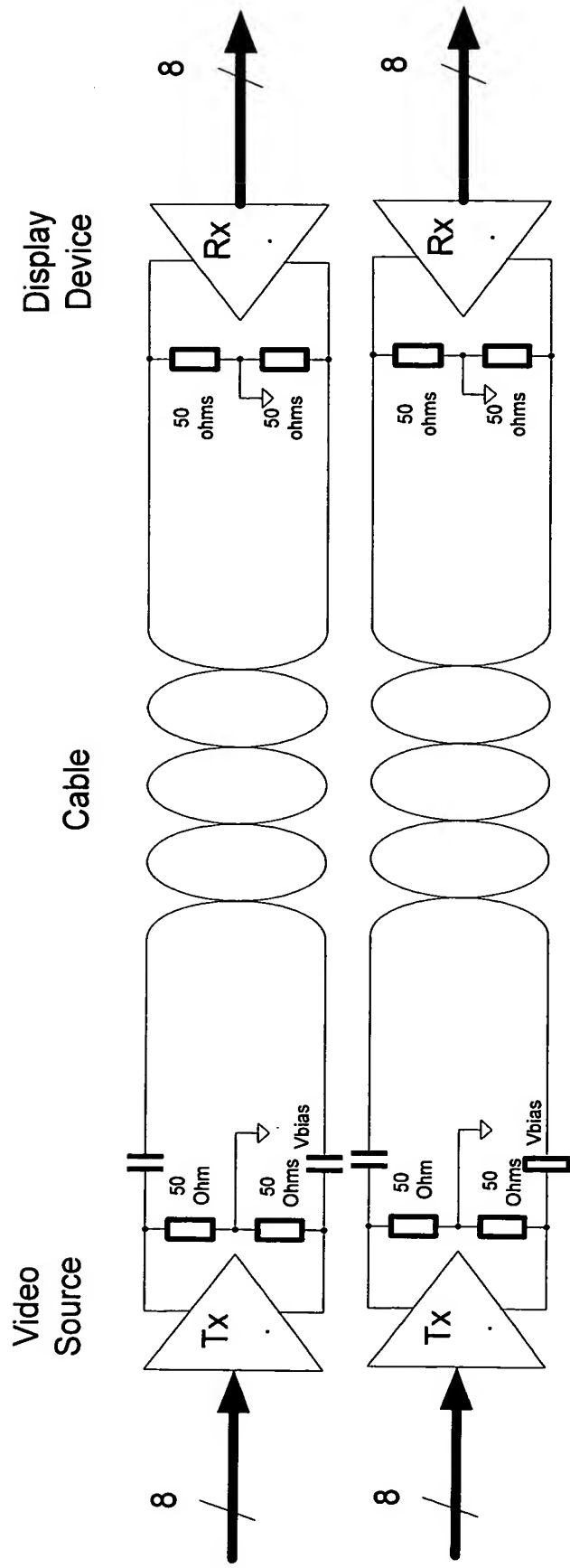


Fig. 16

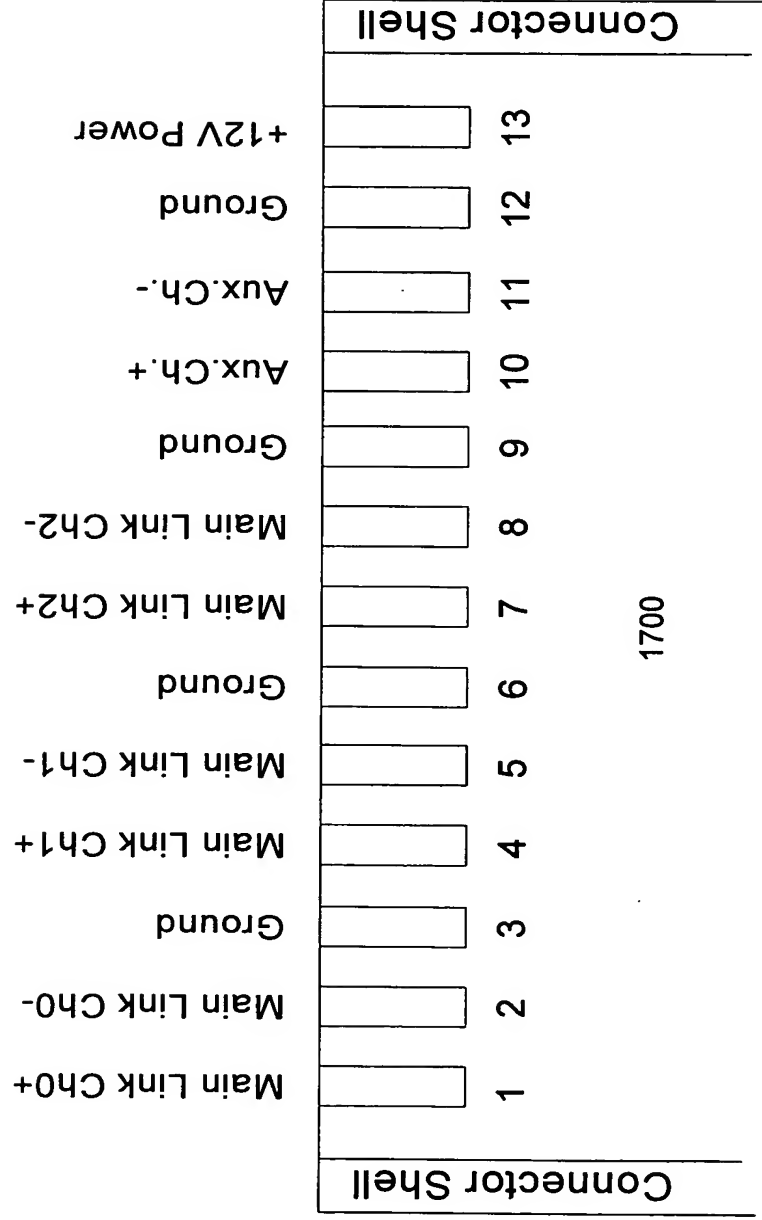


Fig. 17

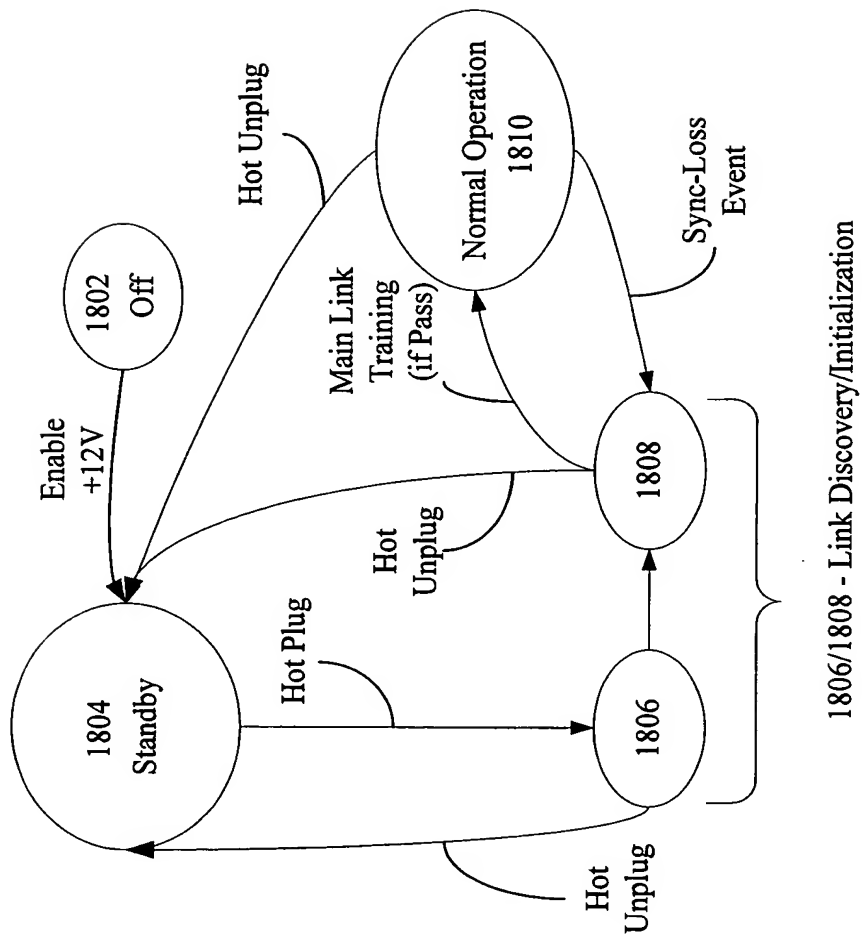


Fig. 18

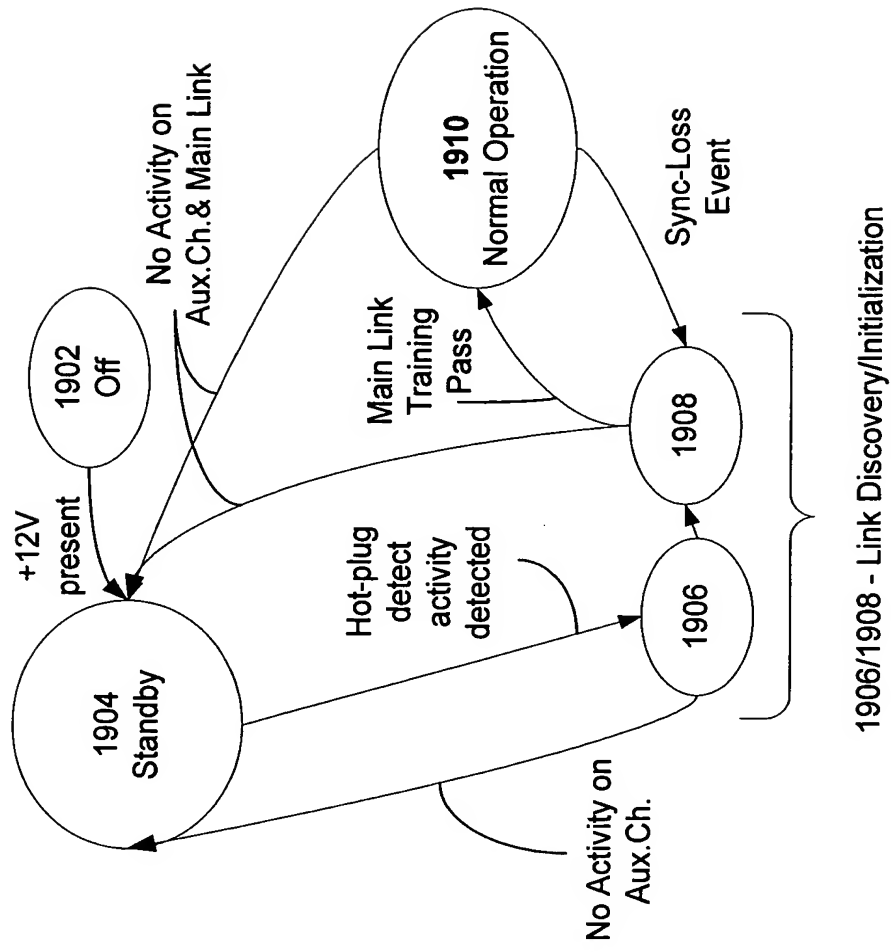
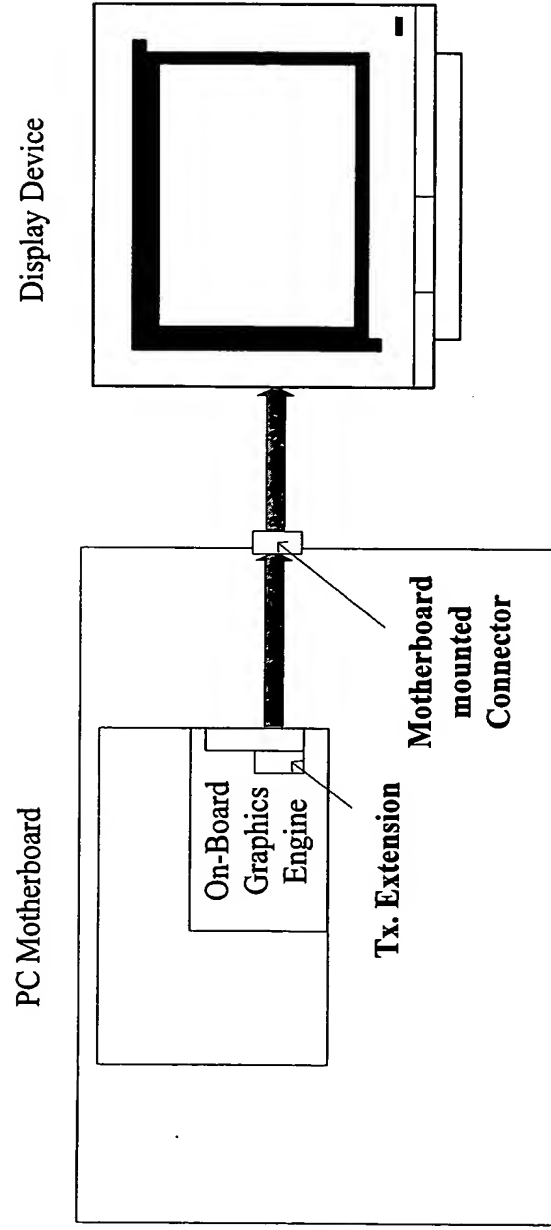


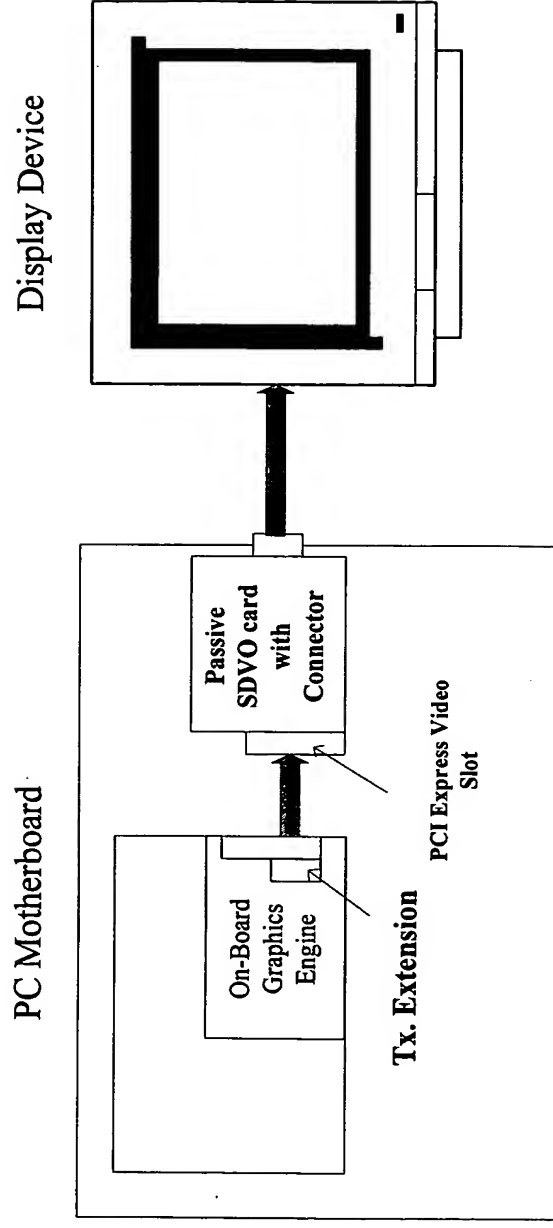
Fig. 19



**PCI EXPRESS MOTHERBOARD WITH DEDICATED DD-  
EXPRESS CONNECTOR**

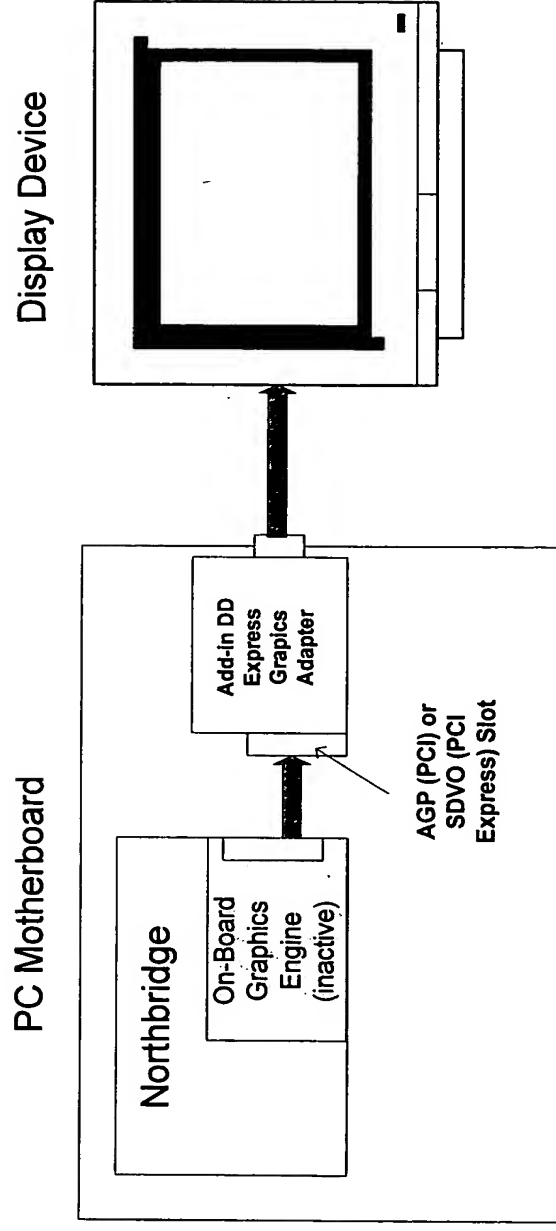
**Fig. 20**





PCI Express motherboard with passive connector card.

Fig. 21



PCI Express motherboard with add-in DD-Express graphics card

Fig. 22

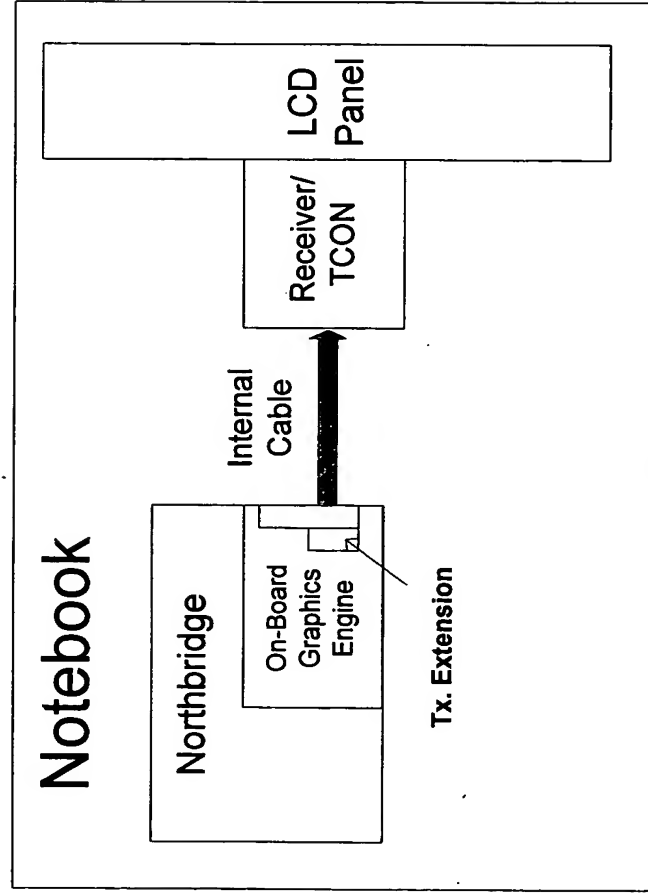
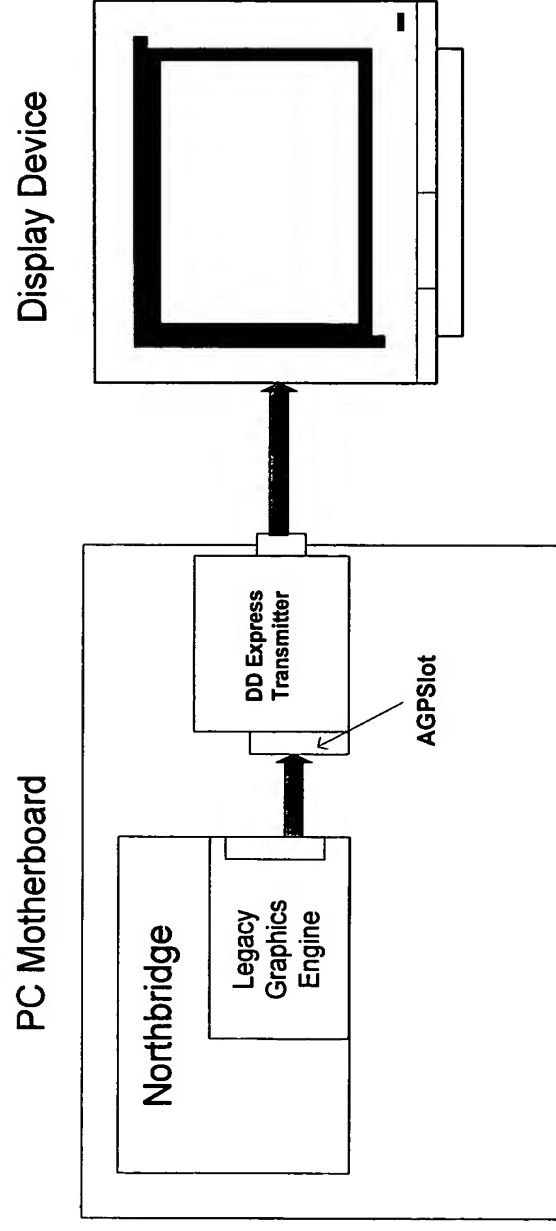


Fig. 23



**Legacy graphics accelerator bus transmitter mounted on a legacy bus card slot converts digital raster data/timing signals into main link streams**

**Fig. 24**

Fig. 25

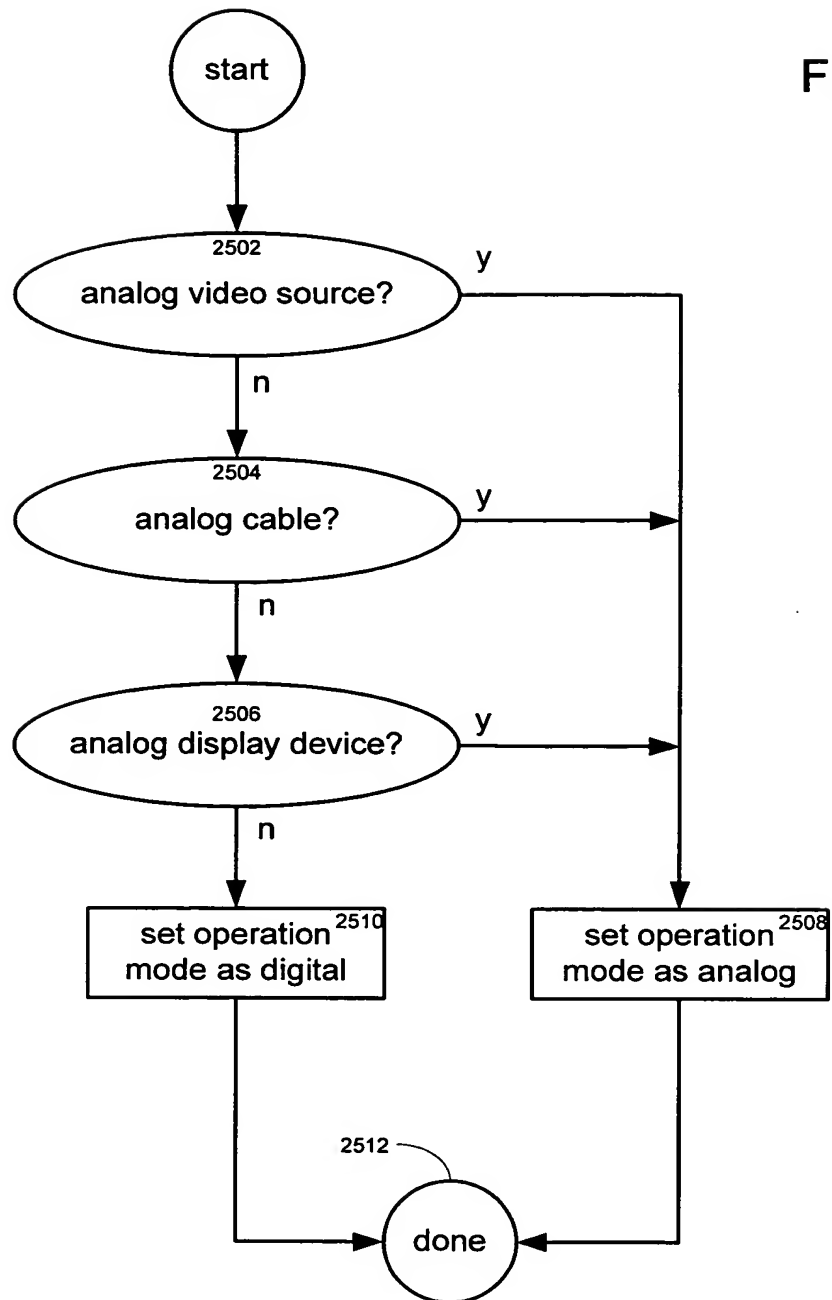
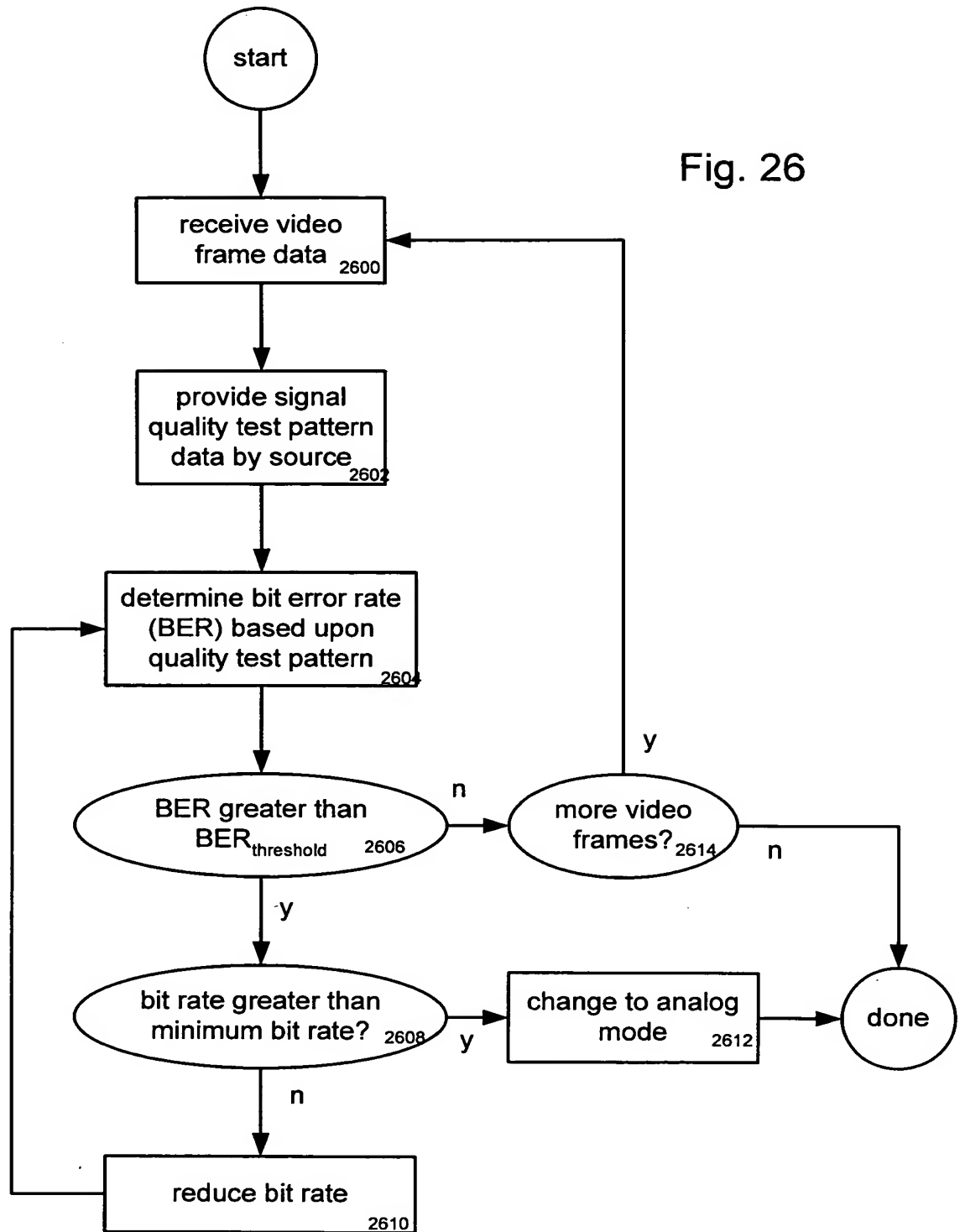


Fig. 26



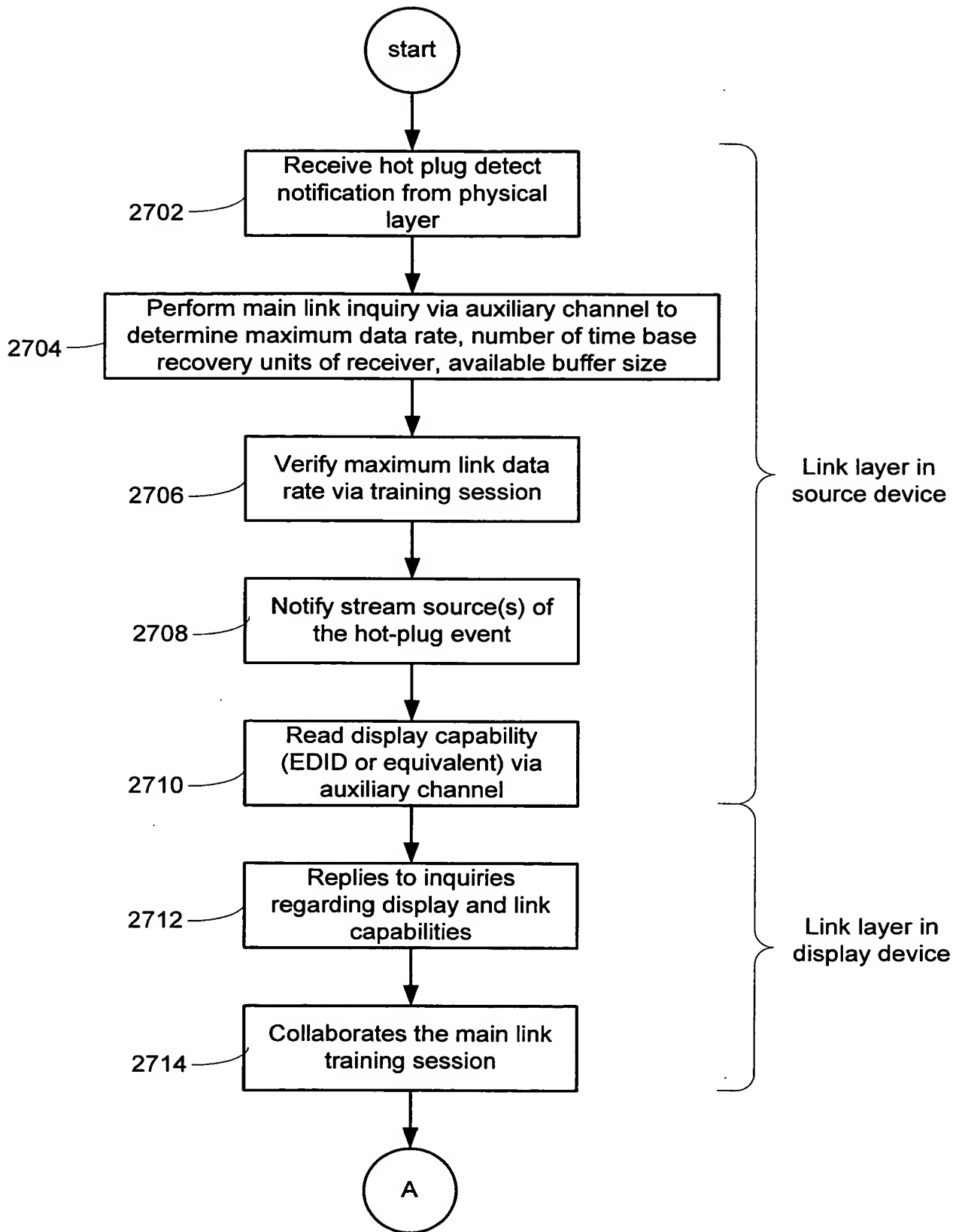


Fig. 27A

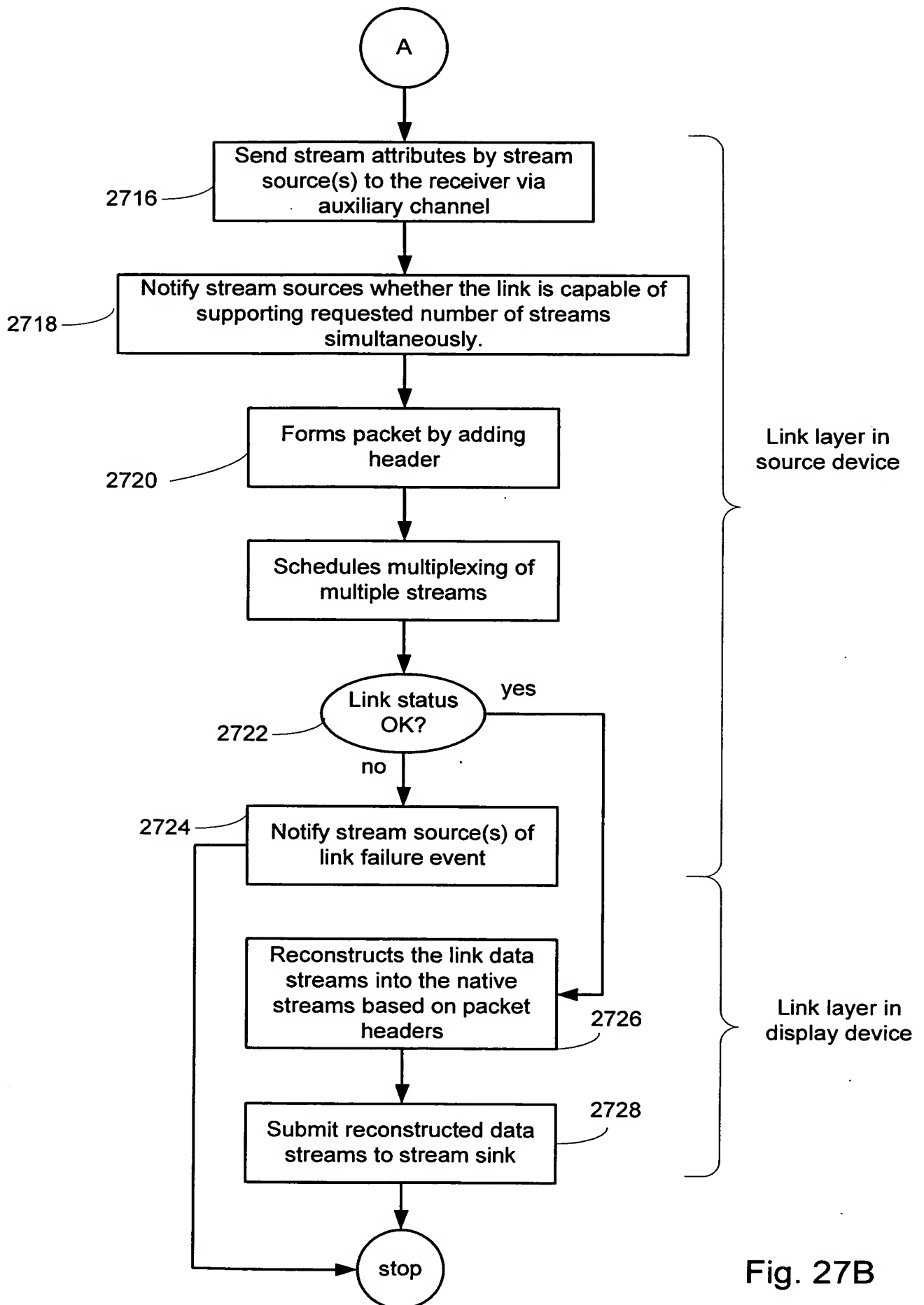


Fig. 27B



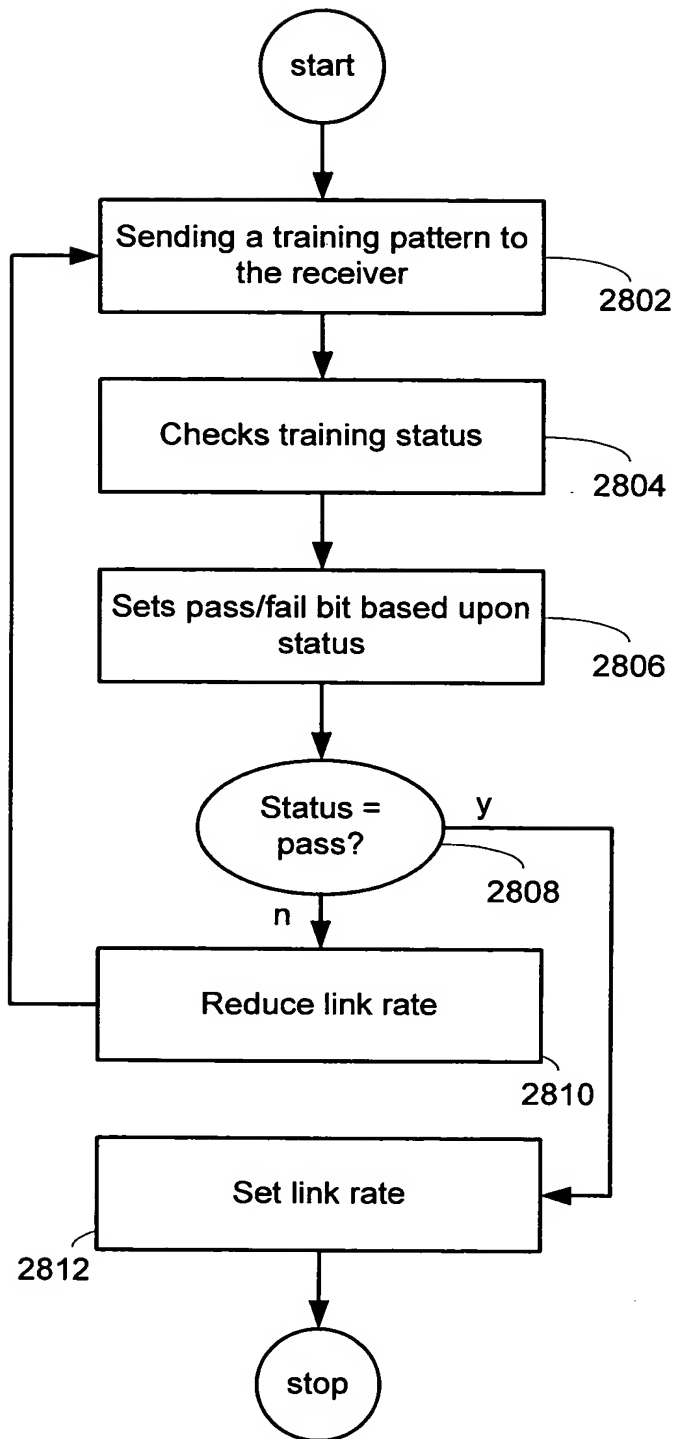


Fig. 28

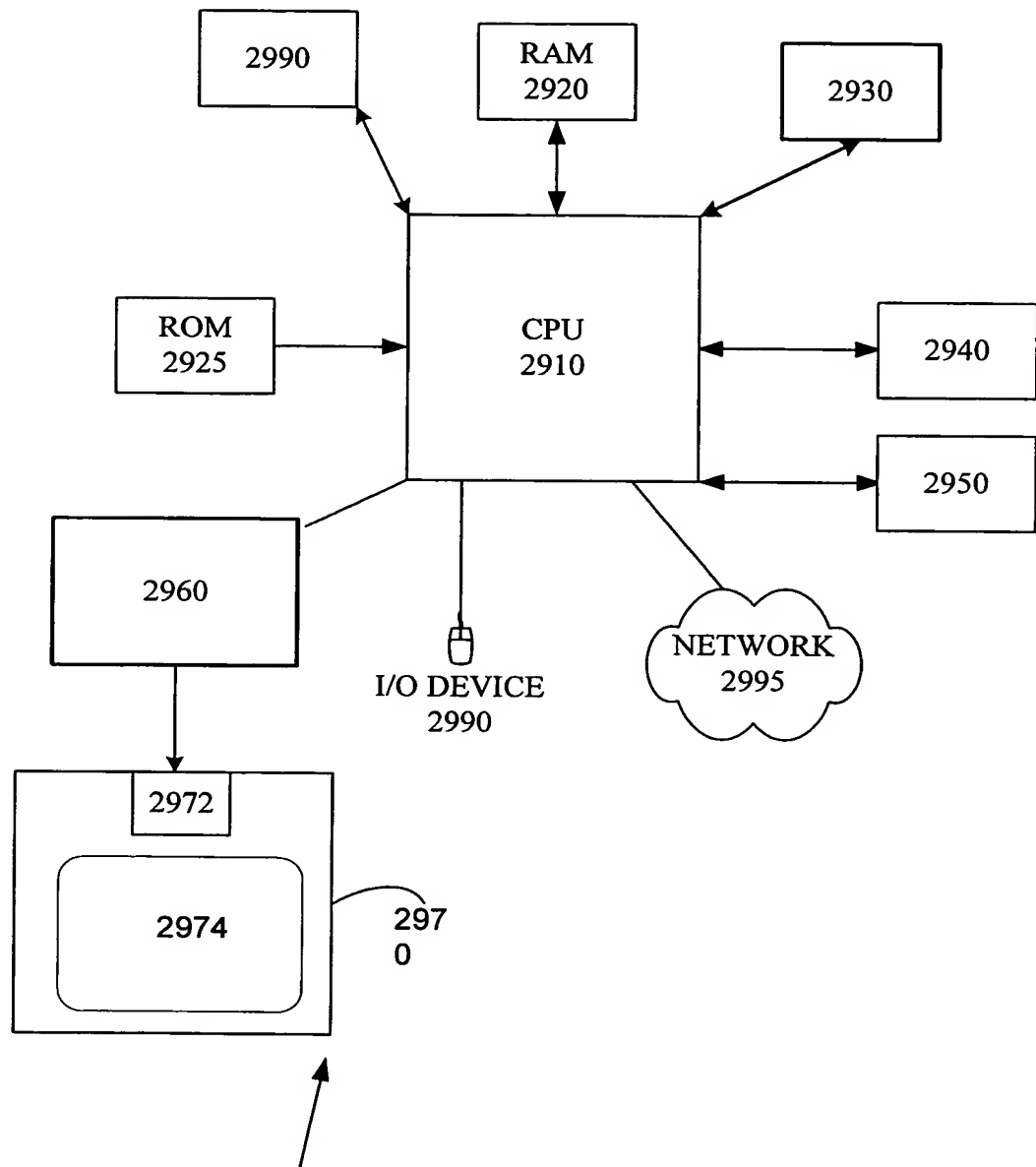


Fig. 29